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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,523	12/03/2003	Bing-Chang Wu	4425-338	3760

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/725,523	WU, BING-CHANG
	Examiner	Art Unit
	Stephen W. Smoot	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 20 June 2005.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The applicant's original disclosure does not provide adequate support for the limitation "a removal rate of said residues of said epitaxial layer on said insulation surface is higher than a removal rate of said epitaxial layer on said semiconductor surface" as set forth in the currently amended version of independent claim 1 (see lines

7-8). Instead, the applicant originally discloses "the removal rate of the insulation surface is faster than the removal rate of the epitaxial layer" or equivalent teachings (see abstract, lines 5-6, see page 2, lines 27-28, page 5, lines 15-17, 25-27, and original claim 1, lines 7-8).

Similarly, the applicant's original disclosure does not provide adequate support for the limitation "wherein a removal rate of said residues of said epitaxial layer on said insulation spacer is higher than a removal rate of said epitaxial layer on said silicon substrate and said upper surface of said polysilicon gate electrode" as set forth in the currently amended version of independent claim 15 (see lines 10-12).

Claims 2-14 are rejected under 35 U.S.C. 112, first paragraph, because they depend on claim 1 and claims 16-17 are rejected under 35 U.S.C. 112, first paragraph, because they depend on claim 15.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Furukawa et al. (US 6,228,728 B1 – reference cited in the prior Office action mailed to applicant on 18 March 2005).

Referring to Figs. 1-3, 13-14, column 11, lines 26-61, and column 14, line 55 to column 15, line 27, Furukawa et al. disclose a method of fabricating a field effect transistor that includes the following features:

- A silicon substrate (1) with silicon oxide trench isolation regions (2) (i.e. insulation devices formed in the substrate) is provided;
- A polysilicon gate electrode (6) is formed on the silicon substrate (1);
- Silicon nitride spacers (9) are formed on sidewalls of the gate electrode (6);
- Epitaxial silicon layers (10) are grown on source/drain regions (7, 8) of the silicon substrate (1) and include the formation of silicon fragments (10a) on the silicon nitride spacers (9);
- The source/drain regions (7, 8) are formed by ion implanting an n-type impurity (i.e. by doping);
- The silicon fragments (10a) are then selectively removed by wet etching in a mixed solution of hydrofluoric acid and nitric acid and, which are removed at a faster etching rate than the epitaxial silicon layers (10) (see column 15, lines 1-3);
- A layer of titanium (22) is then blanket deposited over the epitaxial silicon layers (10) as shown in Fig. 5 (also see column 12, lines 4-14); and

- The titanium layer (22) and the epitaxial silicon layers (10) are then heat treated to form titanium silicide layers (23) by reacting the titanium layer (22) with the epitaxial silicon layers (10) as shown in Figs. 6-7.

These are all of the limitations set forth in claims 1-3, 5-10, 13 of the applicant's invention.

Regarding claims 11-12, Furukawa et al. disclose an alternative embodiment for removing the silicon fragments (10a), featuring an increased etching rate relative to the epitaxial silicon layers (10), by using a plasma that includes a mixture of fluorine and oxygen gases (also see column 16, lines 10-54).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US 6,228,728 B1 – reference cited in the prior Office action mailed to applicant on 18 March 2005) as applied to claims 1-2 above, and further in view of Shishiguchi et al. (US 6,190,976 B1).

As shown above, Furukawa et al. anticipate claims 1-2 of the applicant's invention. However, Furukawa et al. do not teach or suggest forming an epitaxial layer on an upper surface of the gate electrode, which is the further limitation to claim 2 as set forth in claim 4 of the applicant's invention. Further, Furukawa et al. do not teach or suggest using cobalt as the metal, which is the further limitation to claim 1 as set forth in claim 14 of the applicant's invention. Shishiguchi et al. teach the formation of epitaxial silicon on a gate electrode as well as on source/drain regions (see column 6, lines 12-19). Shishiguchi et al. also teach that cobalt can be used as an alternative refractory metal to titanium for forming refractory metal silicides (see column 10, lines 26-30).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Furukawa et al. and Shishiguchi et al. by including the formation of epitaxial silicon on the gate electrode, as taught by Shishiguchi et al., in order to form an electrical contact to the gate electrode because Shishiguchi et al. recognize that silicide contacts have the advantage of reduced contact resistance (see column 2, lines 19-25). It also would have been obvious to substitute cobalt for the titanium metal of Furukawa et al., as taught by Shishiguchi et al., because Shishiguchi et al. recognize that cobalt is known in the art as an alternative refractory metal that can be used for forming silicides (see column 10, lines 26-30).

7. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (US 6,228,728 B1 – reference cited in the prior Office action mailed to applicant on 18 March 2005) in view of Shishiguchi et al. (US 6,190,976 B1).

Referring to Figs. 1-3, 13-14, column 11, lines 26-61, and column 14, line 55 to column 15, line 27, Furukawa et al. disclose a method of fabricating a field effect transistor that includes the following features:

- A silicon substrate (1) is provided;
- A polysilicon gate electrode (6) is formed on the silicon substrate (1);
- Silicon nitride spacers (9) are formed on sidewalls of the gate electrode (6);
- Epitaxial silicon layers (10) are grown on source/drain regions (7, 8) of the silicon substrate (1) and include the formation of silicon fragments (10a) on the silicon nitride spacers (9);
- The silicon fragments (10a) are then selectively removed by wet etching in a mixed solution of hydrofluoric acid and nitric acid and, which are removed at a faster etching rate than the epitaxial silicon layers (10) (see column 15, lines 1-3);
- Alternatively, the silicon fragments (10a) can be removed with an increased etching rate relative to the epitaxial silicon layers (10) by using a plasma that includes a mixture of fluorine and oxygen gases (also see column 16, lines 10-54);
- A layer of titanium (22) is then blanket deposited over the epitaxial silicon layers (10) as shown in Fig. 5 (also see column 12, lines 4-14); and

- The titanium layer (22) and the epitaxial silicon layers (10) are then heat treated to form titanium silicide layers (23) by reacting the titanium layer (22) with the epitaxial silicon layers (10) as shown in Figs. 6-7.

These are limitations set forth in claims 15-17 of the applicant's invention.

However, Furukawa et al. do not teach or suggest forming an epitaxial layer on an upper surface of the gate electrode, which is also a limitation set forth in independent claim 15 of the applicant's invention.

Shishiguchi et al. teach the formation of epitaxial silicon on a gate electrode as well as on source/drain regions (see column 6, lines 12-19).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Furukawa et al. and Shishiguchi et al. by including the formation of epitaxial silicon on the gate electrode, as taught by Shishiguchi et al., in order to form an electrical contact to the gate electrode because Shishiguchi et al. recognize that silicide contacts have the advantage of reduced contact resistance (see column 2, lines 19-25).

Response to Arguments

8. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new grounds of rejection.

Conclusion

9. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER